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EXAMINER	
MISLEH, JUSTIN P	

ART UNIT	PAPER NUMBER
2612	5

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/399,995	PARK, SANG-SIK	
	Examiner	Art Unit	
	Justin P Misleh	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 4 - 20, and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4, 7 - 9, 11 - 15, 17 - 20, and 22* is/are rejected.

7)☒ Claim(s) *5,6,10 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 3 June 2004 have been fully considered but they are not persuasive.

Initially, the Examiner would like to comment on the amendment filed 3 June 2004. The Applicant, *inter alia*, canceled Claims 2 and 3, wherein amended Claim 1 now includes recitations from Claims 2 and 3. Previously, Claim 2 included the following feature: "wherein said input source follower circuit comprises a bias terminal coupled to a power source". Amended Claim 1 does not completely require this feature. Rather, more specifically, amended Claim 1 does not require "a power source"; however does require "a bias terminal of said input source circuit".

The Applicant argues, "that Hynecek does not disclose or suggest all of the recitations of [amended] Claim 1" because "there is no capacitive coupling" between the drain of source follower transistor 52 and the drain of the transistor 50. Rather, the Applicant states that the drain of transistor 52 is "directly (i.e. ohmically) coupled" to the drain of transistor 50.

The Examiner disagrees with the Applicant. Figure 2 clearly shows that the feedback loop begins with the drain of transistor 50 and ends at the drain of transistor 54. As stated in the previous Office Action, the drain of transistor 52 is considered to be a bias terminal of the input source follower circuit (52). Furthermore, turning to column 2 (lines 27 – 32), Hynecek specifically states, "the circuit of Fig. 2 ... provides the advantage[s] of ... positive feedback to the drain transistor 52 which reduces Miller capacitance and improves sensitivity." One with

ordinary skill in the art knows that the Miller effect directly corresponds to the inherent capacitance between terminals in a transistor amplifier (hence the feedback loop), regardless of the actual physical presence of a capacitor. The most important negative effect of Miller's capacitance includes changes in the cutoff frequencies for the various inherent high-pass and low-pass filters in the circuit. Clearly, there are no capacitors in the circuit of Figure 2; however, Hynecek states that a "capacitance", corresponding to Miller's theorem, exists within the circuit of Figure 2. Once again, Hynecek provides the feedback loop to "reduce[s] Miller capacitance and improve[s] sensitivity". If the feedback loop can reduce a "capacitance", then the circuit of figure 2 satisfies the following limitation of amended Claim 1: "an output capacitively connected to a bias terminal of said input source follower circuit."

Furthermore, the Applicant states, "that Claim 20, as amended, is patentable over Hynecek for at least the reasons discussed ... with reference to Claim 1." The Examiner response in regards to amended Claim 1 is also applicable to amended Claim 20.

In regards to Claim 14, the Applicant argues, "the Office Action appears to concede that Hynecek does not disclose the above-highlighted recitations ['operative to variably couple the power source and the bias terminal via a capacitor'], stating 'since the input capacitance of the input source following circuit can be varied by means of the feedback loop along, it is just a design preference to additionally include a capacitor for performing the same' ... the Office Action does not provide any evidence from Hynecek or other prior art of a suggestion or motivation supporting the alleged 'design preference'."

As recited above, in regards to amended Claim 1, the Miller effect directly corresponds to the inherent capacitance between terminals in a transistor amplifier (hence the feedback loop),

regardless of the actual physical presence of a capacitor. The most important negative effect of Miller's capacitance includes changes in the cutoff frequencies for the various inherent high-pass and low-pass filters in the circuit. Clearly, there are no capacitors in the circuit of Figure 2; however, Hynecek states that a "capacitance", corresponding to Miller's theorem, exists within the circuit of Figure 2. Once again, Hynecek provides the feedback loop to "reduce[s] Miller capacitance and improve[s] sensitivity".

The Applicant is claiming, "a feedback circuit connected to said output terminal and to said input source follower circuit and operative to variably couple the power source and the bias terminal via a capacitor"; however, the Examiner believes this is merely a circuit design preference of the Applicant and is not required to achieve the effect of the apparatus. If the feedback loop can reduce a "capacitance", then the circuit of figure 2 satisfies the following limitation of amended Claim 14: "a feedback circuit connected to said output terminal and to said input source follower circuit and operative to variably couple the power source and the bias terminal via a capacitor."

Lastly, the Applicant argues that the dependent claims are patentable at least by virtue of depending from various one of patentable independent Claims 1, 14, and 20. The Examiner has shown that independent Claims 1, 14, and 20 are not patentable; therefore, these arguments are moot.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1, 4, 7 – 9, 11 – 15, 17 – 20, and 22** are rejected under 35 U.S.C. 102(e) as being anticipated by Hynecek.

4. For **Claim 1**, Hynecek discloses, as shown in figure 2 and as stated in columns 1 (lines 10 – 16 and 60- 67) and 2 (lines 1 – 33), an output-compensated buffer (see figure 2), comprising:

a buffer circuit (see figure 2) that receives an input signal (from circuit 55) and produces an output signal responsive thereto at an output terminal (62), said buffer circuit (figure 2) including an input source follower circuit (52) that receives the input signal (from circuit 55); and

a feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) having an input connected to said output terminal (62, by means of circuit 50) and an output capacitively connected to a bias terminal of said input source follower circuit (by means of the drain of the circuit 52) and operative to vary an input capacitance (the input capacitance is provided by the feedback loop, which is connected to the output terminal 62, by means of circuit 50, wherein the output terminal 62 is provided with an input signal, by means of the gate of the circuit 52; thus, varying the input capacitance; also see column 2, lines 27 – 32) of said source follower circuit (52) responsive to the output signal at said output terminal (62).

Figure 2 clearly shows that the feedback loop begins with the drain of transistor 50 and ends at the drain of transistor 54. The drain of transistor 52 is considered to be a bias terminal of the input source follower circuit (52). Furthermore, turning to column 2 (lines 27 – 32), Hynecek specifically states, "the circuit of Fig. 2 ... provides the advantage[s] of ... positive feedback to the drain transistor 52 which reduces Miller capacitance and improves sensitivity." One with ordinary skill in the art knows that the Miller effect directly corresponds to the inherent capacitance between terminals in a transistor amplifier (hence the feedback loop), regardless of the actual physical presence of a capacitor. The most important negative effect of Miller's capacitance includes changes in the cutoff frequencies for the various inherent high-pass and low-pass filters in the circuit. Clearly, there are no capacitors in the circuit of Figure 2; however, Hynecek states that a "capacitance", corresponding to Miller's theorem, exists within the circuit of Figure 2. Once again, Hynecek provides the feedback loop to "reduce[s] Miller capacitance and improve[s] sensitivity". If the feedback loop can reduce a "capacitance", then the circuit of figure 2 satisfies the following limitation of amended Claim 1: "an output capacitively connected to a bias terminal of said input source follower circuit."

5. As for **Claim 4**, Hynecek discloses, an output-compensated buffer according to Claim 1, wherein said feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) is operative to variably capacitively couple the bias terminal (the drain of the circuit 52) to the power source (VDD) responsive to the output signal at the output terminal (62).

As stated in column 2 (lines 27 – 32), the input capacitance is provided by the feedback loop, which is connected to the output terminal (62), by means of circuit (50), wherein the output

terminal (62) is provided with an input signal, by means of the gate of the circuit 52; thus, varying the input capacitance.

6. As for **Claim 7**, Hynecek discloses, an output-compensated buffer according to Claim 1, wherein said source follower circuit (52) comprises:

a first transistor (52) having a source terminal, a gate terminal configured to receive the input signal (from circuit 55), and a drain terminal connected to the power source (VDD) through a resistor (64); and

a second transistor (54) having a drain terminal connected to the source terminal of the first transistor (by means of the node supplying an input signal to the circuit 50), a source terminal connected to a signal ground (clearly shown in figure 2) and a gate terminal configured to receive a control signal (initially, a gate terminal of a transistor is always configured to receive a control signal as it the means that controls the transistor; moreover a control signal is supplied constant current source 60); and

wherein said feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) is coupled to the drain terminal of said first transistor.

7. As for **Claim 8**, Hynecek discloses, an output-compensated buffer according to Claim 7, wherein said feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) is capacitively coupled the bias terminal (the drain of the circuit 52).

As stated in column 2 (lines 27 – 32), the input capacitance is provided by the feedback loop, which is connected to the output terminal (62), by means of circuit (50), wherein the output

terminal (62) is provided with an input signal, by means of the gate of the circuit 52; thus, varying the input capacitance.

8. As for **Claim 9**, Hynecek discloses, an output-compensated buffer according to Claim 8, wherein said feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) is operative to variably capacitively couple the bias terminal (the drain of the circuit 52) to the power source (VDD) responsive to the output signal at the output terminal (62).

As stated in column 2 (lines 27 – 32), the input capacitance is provided by the feedback loop, which is connected to the output terminal (62), by means of circuit (50), wherein the output terminal (62) is provided with an input signal, by means of the gate of the circuit 52; thus, varying the input capacitance.

9. As for **Claim 11**, Hynecek discloses, an output-compensated buffer according to Claim 1, wherein the output terminal (62) of the buffer circuit (see figure 2) is an output terminal of the source follower circuit.

10. As for **Claim 12**, Hynecek discloses, an output-compensated buffer according to Claim 1, wherein the buffer circuit (figure 2) further comprises a source follower circuit (54) connected to an output (the output and the source of the circuit 52 and the drain of the circuit 54 are the same node) of the input follower circuit (52) and operative to produce the output signal responsive to the inputs signal (from circuit 55) applied the input source follower circuit (52).

11. As for **Claim 13**, Hynecek discloses, an output-compensated buffer according to Claim1, in combination with a CCD image capture device (inherent; see explanation below), wherein the

CCD image capture device includes a horizontal transfer section that generates the input signal (included in the inherency above).

While Hynecek does not show the details of a CCD imager, the amplifier disclosed by Hynecek clearly designed for and directly used by CCD imager sensors. Therefore, it is inherent that a CCD exists and includes the horizontal transfer section; otherwise, the amplifier of Hynecek would be rendered inoperable.

12. As for **Claim 18**, Hynecek discloses, an output-compensated buffer according to Claim13, wherein the buffer circuit (figure 2) further comprises a source follower circuit (54) connected to an output (the output and the source of the circuit 52 and the drain of the circuit 54 are the same node) of the input follower circuit (52) and operative to produce the output signal responsive to the inputs signal (from circuit 55) applied the input source follower circuit (52).

13. For **Claim 14**, Hynecek discloses, as shown in figure 2 and as stated in columns 1 (lines 10 – 16 and 60- 67) and 2 (lines 1 – 33), an output-compensated buffer (see figure 2), comprising:

a buffer circuit (see figure 2) that receives an input signal (from circuit 55) and produces an output signal responsive thereto at an output terminal (62), said buffer circuit (figure 2) including an input source follower circuit (52) that receives a bias voltage from a power source (VDD); and

a feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) connected to said output terminal (62, by means of circuit 50) and to said input source follower circuit (by means of the drain of the circuit 52) and operative to variably couple the

power source (VDD) and the bias terminal (the drain of circuit 52) via a capacitor (this is a design preference; see explanation below).

The input capacitance is provided by the feedback loop, which is connected to the output terminal 62, by means of circuit 50, wherein the output terminal 62 is provided with an input signal, by means of the gate of the circuit 52; thus, varying the input capacitance; also see column 2, lines 27 – 32. Therefore, since the input capacitance of the input source follower circuit can be varied by means of the feedback loop alone, it is just a design preference to additionally include a capacitor for performing the same.

The most important negative effect of Miller's capacitance includes changes in the cutoff frequencies for the various inherent high-pass and low-pass filters in the circuit. Clearly, there are no capacitors in the circuit of Figure 2; however, Hynecek states that a "capacitance", corresponding to Miller's theorem, exists within the circuit of Figure 2. Once again, Hynecek provides the feedback loop to "reduce[s] Miller capacitance and improve[s] sensitivity".

The Applicant is claiming, "a feedback circuit connected to said output terminal and to said input source follower circuit and operative to variably couple the power source and the bias terminal via a capacitor"; however, the Examiner believes this is merely a circuit design preference of the Applicant and is not required to achieve the effect of the apparatus. If the feedback loop can reduce a "capacitance", then the circuit of figure 2 satisfies the following limitation of amended Claim 14: "a feedback circuit connected to said output terminal and to said input source follower circuit and operative to variably couple the power source and the bias terminal via a capacitor."

14. As for **Claim 15**, Hynecek discloses, an output-compensated buffer according to Claim 14, wherein said source follower circuit (52) comprises:

a first transistor (52) having a source terminal, a gate terminal configured to receive the input signal (from circuit 55), and a drain terminal connected to the power source (VDD) through a resistor (64); and

a second transistor (54) having a drain terminal connected to the source terminal of the first transistor (by means of the node supplying an input signal to the circuit 50), a source terminal connected to a signal ground (clearly shown in figure 2) and a gate terminal configured to receive a control signal (initially, a gate terminal of a transistor is always configured to receive a control signal as it the means that controls the transistor; moreover a control signal is supplied constant current source 60); and

wherein said feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) is coupled to the drain terminal of said first transistor.

15. As for **Claim 17**, Hynecek discloses, an output-compensated buffer according to Claim 14, wherein the output terminal (62) of the buffer circuit (see figure 2) is an output terminal of the source follower circuit.

16. As for **Claim 19**, Hynecek discloses, an output-compensated buffer according to Claim14, in combination with a CCD image capture device (inherent; see explanation below), wherein the CCD image capture device includes a horizontal transfer section that generates the input signal (included in the inherency above).

While Hynecek does not show the details of a CCD imager, the amplifier disclosed by Hynecek clearly designed for and directly used by CCD imager sensors. Therefore, it is inherent that a CCD exists and includes the horizontal transfer section; otherwise, the amplifier of Hynecek would be rendered inoperable.

17. For **Claim 20**, Hynecek discloses, as shown in figure 2 and as stated in columns 1 (lines 10 – 16 and 60- 67) and 2 (lines 1 – 33), an image capture device, comprising:

a charged coupled device (CCD) that generates a video signal (inherent; see explanation below);

a buffer circuit (see figure 2) responsive to the CCD and operative to receives the video signal that receives an input signal (included with the inherency above) and produce an output signal (amplified signal) responsive thereto at an output terminal (62), said buffer circuit including an input source follower circuit (52) that receives the input signal (by means of the gate of circuit 52); and

a feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) having an input connected to said output terminal (62, by means of circuit 50) and an output capacitively coupled to a bias terminal said input source follower circuit (by means of the drain of the circuit 52) and operative to vary an input capacitance (the input capacitance is provided by the feedback loop, which is connected to the output terminal 62, by means of circuit 50, wherein the output terminal 62 is provided with an input signal, by means of the gate of the circuit 52; thus, varying the input capacitance; also see column 2, lines 27 – 32) of said source follower circuit (52) responsive to the output signal at said output terminal (62).

While Hynecek does not show the details of a CCD imager, the amplifier disclosed by Hynecek clearly designed for and directly used by CCD imager sensors. Therefore, it is inherent that a CCD exists; otherwise, the amplifier of Hynecek would be rendered inoperable.

Figure 2 clearly shows that the feedback loop begins with the drain of transistor 50 and ends at the drain of transistor 54. The drain of transistor 52 is considered to be a bias terminal of the input source follower circuit (52). Furthermore, turning to column 2 (lines 27 – 32), Hynecek specifically states, "the circuit of Fig. 2 ... provides the advantage[s] of ... positive feedback to the drain transistor 52 which reduces Miller capacitance and improves sensitivity." One with ordinary skill in the art knows that the Miller effect directly corresponds to the inherent capacitance between terminals in a transistor amplifier (hence the feedback loop), regardless of the actual physical presence of a capacitor. The most important negative effect of Miller's capacitance includes changes in the cutoff frequencies for the various inherent high-pass and low-pass filters in the circuit. Clearly, there are no capacitors in the circuit of Figure 2; however, Hynecek states that a "capacitance", corresponding to Miller's theorem, exists within the circuit of Figure 2. Once again, Hynecek provides the feedback loop to "reduce[s] Miller capacitance and improve[s] sensitivity". If the feedback loop can reduce a "capacitance", then the circuit of figure 2 satisfies the following limitation of amended Claim 20: "an output capacitively connected to a bias terminal of said input source follower circuit."

18. As for **Claim 22**, Hynecek discloses, an image capture device according to Claim 20, wherein said feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a

resistor 64) is operative to variably capacitively couple the bias terminal (the drain of the circuit 52) to the power source (VDD) responsive to the output signal at the output terminal (62).

As stated in column 2 (lines 27 – 32), the input capacitance is provided by the feedback loop, which is connected to the output terminal (62), by means of circuit (50), wherein the output terminal (62) is provided with an input signal, by means of the gate of the circuit 52; thus, varying the input capacitance.

Allowable Subject Matter

19. **Claims 5, 6, 10, and 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. For **Claims 5 and 16**, while the prior art teaches of an output-compensated buffer comprised of a buffer circuit including an input source follower circuit that receives an input signal and a feedback circuit connected to an output terminal and to the input source follower circuit that is operative to vary an input capacitance of the source follower circuit wherein the bias terminal of the input source follower circuit is coupled to a power source and wherein the feedback circuit is variably capacitively coupled the power source and the bias terminal; however, the prior art does not teach or fairly suggest wherein the feedback circuit comprises a second source follower circuit having an input terminal that receives an output signal output from the input source follower circuit and an output terminal that is coupled to the bias terminal of the input source follower circuit.

21. For **Claim 10**, while the prior art teaches of an output-compensated buffer comprised of a buffer circuit including an input source follower circuit that receives an input signal and a feedback circuit connected to an output terminal and to the input source follower circuit wherein the input source follower circuit is comprised of a first transistor having a source terminal, a gate terminal configured to receive the input signal, and a drain terminal connected to the power source through a resistor and a second transistor having a drain terminal connected to the source terminal of the first transistor, a source terminal connected to a signal ground and a gate terminal configured to receive a control signal; and wherein said feedback circuit is coupled to the drain terminal of said first transistor; however, the prior art does not teach or fairly suggest wherein the feedback circuit comprises a third transistor having a source terminal, a drain terminal connected to the power source, and a gate terminal connected to the output terminal of the buffer circuit and a fourth transistor having a drain terminal connected to the source terminal of the third transistor, a drain terminal connected to a signal ground and a gate terminal configured to receive a control signal; and a capacitor coupled between the drain terminal of the fourth transistor and the drain terminal of the first transistor.

Conclusion

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 703.305.8090. The Examiner can normally be reached on Monday through Thursday from 7:30 AM to 5:30 PM and on alternating Fridays from 7:30 AM to 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wendy R Garber can be reached on 703.305.4929. The fax phone number for the organization where this application or proceeding is assigned is 703.872.9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
SEPTEMBER 7, 2004

NGOC-YEN VU
PRIMARY EXAMINER